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Design of Binary Adders by Using Quantum Cellular Automata Technique

K. P. Jamunalaksmi[1], M. Mohanapriyaa[2]
Assistant Professor, Adithya Institute of Technology
Assistant Professor, Adithya Institute of Technology

Abstract: Now a days transistor size become reduced as much as possible. The new rising technologies, with low area/power/latency properties, are gaining momentum as replacements for CMOS. In particular, for quantum dot cellular automata (QCA) realization, many arithmetic circuits have been redesigned .This technique overcome the sizing problem of the IC The basic QCA elements are a 3-way majority gate and an inverter.

Keywords: QCA, Carry look ahead adder, MODELSIM

I. Introduction

In this paper, QCA decimal full adder that is mostly composed of fully utilized majority gates, and rarely includes PUMs. The proposed circuit has been designed and tested by Xilinx Tool and compared with relevant Normal architecture, where the cell count, area and delay improvement, respectively. The Proposed design is done by Verilog HDL and Simulated by Modelsim 6.4 c and it is implemented in FPGA Spartan 3 XC3S 200 TQ-144. In Existing system one-bit QCA adder structure is based on a new algorithm that for QCA addition it requires only three majority gates and two inverters. By connecting n one-bit QCA adders, can obtain an n-bit carry look-ahead adder with the reduced Hardware, while retaining the simple clocking scheme and parallel structure of the original carry look-ahead adder approach. This type of adder design follows that for a conventional ripple carry adder, but with a new layout optimized to QCA technology. It shown that a very high delay can be obtained with an optimized layout. This type of adder is in contrast with the conventional ripple carry adder. To avoid this type of confusion, the new layout is referred to as the Carry Flow Adder (CFA) here. In this Carry Flow Adder, it occupies more Number of gate Counts and it creates more Delay. In this desgin, a novel QCA adder design has been presented that it reduces the number of QCA cells in comparison to previously reported designs. In order to obtain n-bit carry look ahead adder with the reduced Hardware, n proposed one bit QCA adders can be connected. while retaining the simple clocking scheme and parallel structure of the original carry look-ahead adder approach A QCA decimal full adder that is mostly composed of fully utilized majority gates and rarely includes PUMs. The proposed circuit has been designed. Modified version of older Conventional Eqn.

$s_0 = w_0$, $s_1 = \mathcal{M}(\overline{w_1}, w_4\overline{w_1}, w_3w_2) \vee \overline{w_4 \vee w_3}w_1$,
$s_2 = \mathcal{M}(w_4 \vee w_1, \overline{w_3}w_2, w_2 \vee \overline{w_1})$, $s_3 = \mathcal{M}(\overline{w_2}, w_4w_1, w_3\overline{w_1})$,
$c_{out} = \mathcal{M}\big(w_4, w_3 \vee w_4, \mathcal{M}(w_1, w_2, w_3)\big)$

II. Quantum Cellular Automata

Booth-encoded sign-digit-based conditional probability (BSCP) method

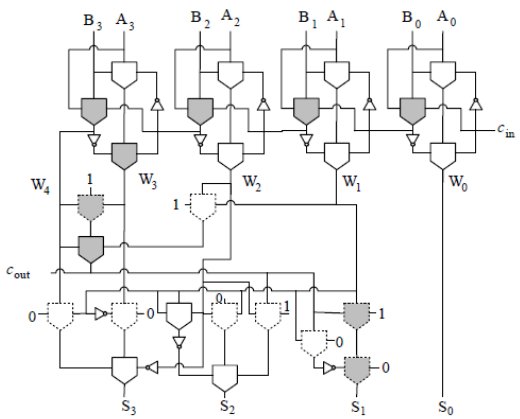

Fig1: DFA with 16 fully- and 9 partially-utilized M gate

Quantum Cellular Automata (QCA) is a method it refers to the models of quantum computation, and it have been devised to the conventional models of cellular automata in analogy introduced by von Neumann. It may also refer to quantum dot cellular automata, by exploiting quantum mechanical phenomena which is a proposed for physical implementation of "classical" cellular automata. Quantum Cellular Automata is a method has attracted a lot of attention as a result of its extremely small feature size at the molecular or even atomic scale and its ultra-low power consumption, making it one candidate for replacing CMOS type of technology.

The following are the features of models of quantum cellular automata:
i) The computation has been considered to come about by the parallel operation of multiple computing devices, or cells. The cells are usually considered to be identical and it has finite-dimensional quantum systems.
ii) Each cell has a neighborhood of other cells. Altogether these form a network of cells, which is usually taken to be regular.
iii) The evolution of all of the cells has a number of physics-like symmetries. Locality is one: the next state of a cell depends only on its current state and that of its neighbors. Homogeneity is another method and the evolution acts the same everywhere, and is independent of time.

• The state space of the cells, and the operations performed on them, it should be motivated by the principles of quantum mechanics.

Any particular device designed in order to represent the data and perform computation, regardless of the physics principles it exploits all the materials used in order to build it. Device must have two fundamental properties: distinguish ability and conditional change of state, the latter implying the former. This means that such a that make in order to distinguish between states device must have barriers, and that perform conditional change of the state it should have the ability to control these type of barriers. Let us consider in a digital electronic system, transistors play the important role of such type of controllable energy barriers, making it extremely practical to perform computing with them.

A QCA cell can be viewed as a set of four charge containers (or “dots”) positioned at the corners of a square. The QCA cell contains two extra mobile electrons that it is not in cells but it can quantum mechanically tunnel between dots. The electrons are forced to the antipodal corner positions by Coulomb repulsion. If the two extra electrons are completely localized on dots 1 and 3, the polarization is + 1 (binary 1); if they are localized on dots 2 and 4, the polarization is −1 (binary 0). Informations are transferred by the given electrical current in conventional type of logic circuits, QCA operates by the Coulombic type of interaction with neighbours by connects the state of one cell to the state . The configuration of the polarization of a set of cells reflects the lowest energy state (ground state). This results in a technology in which information transfer (interconnection) is the same as information transformation (logic manipulation) with low-power dissipation.

III. QCA Cell Model

Isolated QCA Cell

A QCA contains four quantum dots aligned in a square area separated by a distance, sufficient enough for the electrons to tunnel from one dot to another. Initially all the four dots contain equal number of electrons. Later two extra electrons are added in any two quantum dots of the cell. These two extra electrons settle down at the diagonals of the QCA cell because of the coulombic repulsion. Depending on which diagonal the electrons rests, call the cell has either Positive polarity or a negative polarity. These two polarities can be used to represent a 0 or a 1 which are the two basic requirements of a Digital world.

IV. Cell - Cell Coupling

The electrons tunnel only through Quantum dots within the cell. They do not tunnel between the Quantum dots of adjacent cells. Polarity of a QCA Cell is influenced by the polarity of the nearby cells. The abruptness of cell-cell response function depends on the ratio of strength of tunneling energy to coulomb energy of electrons on neigh bouring cells. By fixing the polarization of cell 1, the columbic effect on the polarization of cell2 is measured. By changing the polarization of cell 1 from -1 to +1 the columbic effect of it on polarization of cell2 is observed .This nonlinearity 13 and bi stable saturation of this response is same as gain of a conventional buffer in a CMOS technology.

V. ModelSim

ModelSim SE is a platform it has most powerful in Linux, UNIX , Windows-based simulation and debug environment, it combines high performance and in the modern industry intuitive GUI · Improved FSM type machines debug options and it includes control of basic information, transition table and warning

messages. Added support of given FSM Multi-state transitions coverage (i.e. coverage for all possible FSM state sequences).

· Improved debugging with hyperlinked navigation between the objects and their declaration, and between visited source files.

· The dataflow window is used to compute and display all the paths from one net to another net

· Enhanced code coverage of the data management with fine grain control of information in the source window.

· Toggle coverage has been enhanced in order to support the System Verilog types: structures, packed unions, fixed-size multi-dimensional arrays and real. Some IEEE VHDL 2008 features are hereby supported including source code encryption. With support of new VPI types, including packed arrays of struct nets and variables.

VI. High-Performance, Scalable Simulation Environment

ModelSim provides a scalable and seamless, performance and capabilities. The use of a single compiler and library system for all ModelSim configurations, employing the right ModelSim configuration for project needs is that simple as pointing in the given environment to the appropriate installation directory in the platform.

ModelSim also supports while maintaining high performance very fast time-tenet-simulation turnarounds with its new black box use model, known as bbox. With bbox, non-changing elements are to be compiled and optimized once and reused while running a modified version of the test bench. bbox it delivers dramatic throughput improvements of up to 3X when running a large suite of test cases in software.

VII. Results

The proposed addition architecture is implemented for using the QCA Designer tool adopting the same rules and simulation settings used.

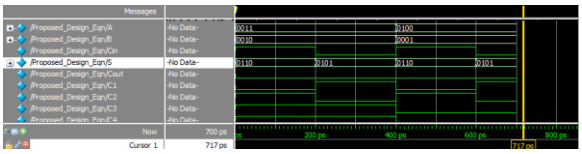

Fig2: QCA Output

Proposed Design Equation Decimal

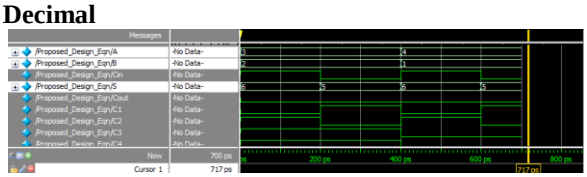

Fig 3: Output in decimal STOP WATCH BASED ON QCA ADDER

VIII. Device Utilization Summary

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	14	3,840	1%	
Logic Distribution				
Number of occupied Slices	8	1,920	1%	
Number of Slices containing only related logic	8	8	100%	
Number of Slices containing unrelated logic	0	8	0%	
Total Number of 4 input LUTs	14	3,840	1%	
Number of bonded IOBs	14	97	14%	
Total equivalent gate count for design	87			
Additional JTAG gate count for IOBs	672			

Majority gate is the basic QCA component that together with inverter gate constitute a complete logic set, since AND and OR gates can be defined in terms of partially utilized majority gate, where one input is 0 and 1, respectively. Many logical circuits that have been realized in CMOS, including those of computer arithmetic circuits are also realized in QCA platform. Instead of trivial mapping of AND/OR gates to partially utilized majority gates, one can reformulate the logical expressions of the corresponding Digital designs in terms of maximizing the use of fully utilized majority gates. This is generally expected to lead to less number of total majority gates, as is the case in the design of binary full adders with only 3 majority gates. Several previous attempts for QCA implementation of decimal full adders (DFA) have led to rather inefficient designs, where the number of partially utilized majority gates is considerably more than that of fully utilized ones. With careful examination of the DFA logical equations. The Digital Watch based on binary adder designed as described in

this brief exhibited a delay clock cycles, occupied an active area, and achieved an ADP. Finally we will implement the QCA DFA Adder and it will used in Digital stop watch Design.

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