# PERFORMANCE OF THREE PHASE 11-LEVEL INVERTER WITH REDUCED NUMBER OF SWITCHES USING DIFFERENT PWM TECHNIQUES

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**ABSTRACT**: As compared to conventional inverter topologies like diode clamped and capacitor clamped inverters, the cascaded multilevel inverter has lesser harmonics as well as lower switching stress. The cascaded topology has more number of power switches leading to greater heat losses, larger size, higher cost and more gate drive circuitry. The proposed configuration contains less number of switches and produces lesser harmonics in the output voltage than the cascaded topology. A comparison between four different types of pulse width modulation (PWM) techniques, namely, In-phase disposition (IPD), Anti-phase disposition (APD), Carrier Overlap (CO) and Variable Frequency (VF) PWM methods, has been done. The results have been verified through simulation study in MATLAB/Simulink in order to select the best PWM method that provides minimum THD in the output voltage. An LC filter has been designed to improve the harmonic profile.

**Keywords:** Multilevel inverter, PWM technique, total harmonic distortion, LC filters.

## I INTRODUCTION

Power electronic devices play a major role in the conversion and control of electric power, especially to extract power from renewable energy sources like photovoltaic array and wind energy [1]. Conversion of DC to AC power can be done with the help of inverters (single phase or three phases). Conventional bipolar inverters produce alternating staircase waveforms with higher harmonics. Thus, the multilevel inverters (MLI) were developed [2]. This paper provides a new three phase configuration to produce the II-level output with less total harmonic distortion (THD) in its output voltage. IPD, APD, CO and VF PWM techniques were used to produce switching pulses [3].

The cascaded H-bridge (CHB) configuration has lesser number of components as compared to the conventional diode clamped or capacitor clamped inverters [4]. It contains single phase inverters connected in series with separate DC sources that can be derived from renewable energy sources like solar PV cell, bio fuel cell or wind turbine [5]. Each single phase inverter produces two DC voltage levels. Bridges with separate DC sources are cascaded to each other for more DC levels. The switches operate at fundamental frequency of 50Hz.

The diode clamped MLI has 20 switches, 90 diodes and 10 main DC-bus capacitors per phase to produce an 11- level staircase as the output voltage. The capacitor clamped MLI uses 20 switches, 45 clamping capacitors and 10 main DC-bus capacitors per phase whereas the cascaded H-bridge inverter uses only 24 switches per phase to produce the same output [6-7]. This paper describes a single phase inverter configuration with eight switches and three DC sources. A three phase multilevel inverter is obtained by interconnecting three single phase inverters to a star connected pure resistive load with a common earth point. Therefore, this circuit offers lesser gate control circuitry, lesser cost, lesser heating, more ease of installation and lesser electromagnetic interference. Table.I shows the comparison of the number of components between different topologies. The performance of the inverter using IPD, APD, CO and VF PWM methods is shown [8]. A passive series LC filter is designed to produce a sine wave from the staircase inverter output. The purpose of the output LC filter is attenuating voltage ripples due to the inverter switching [9].

This paper is organized into many sections. Section II contains the circuit configuration and its modes of operation. Section III mentions some modulation schemes available for switching of the inverter. The simulation results are analyzed in section IV. The waveform obtained after implementing the series LC filter at the inverter output is analyzed in section V. Section VI gives the conclusion.

TABLE. I
NUMBER OF COMPONENTS PER PHASE FOR DIFFERENT 11-LEVEL INVERTER TOPOLOGIES

| Sl.No. | Configuration | Number of switches per phase | Number of conducting switches per phase |
|--------|---------------|------------------------------|-----------------------------------------|
| 1 | Diode Clamped | 20 | 4 |
| 2 | Capacitor Clamped | 20 | 4 |
| 3 | Cascaded H-Bridge | 24 | 14 |
| 4 | Eight switch type | 8 | 4 |

## II    PROPOSED TOPOLOGY AND ITS OPERATION

The proposed inverter configuration has eight switches and three DC sources per phase as shown in Fig.l. The series combination among the three DC sources V dc, 2V dc and 2V dc can be used to produce eleven DC levels at the inverter output in a single cycle. Fig.2 provides the simulation circuit of the proposed single phase circuit in MA TLAB. In each mode, four of the switches operate simultaneously.
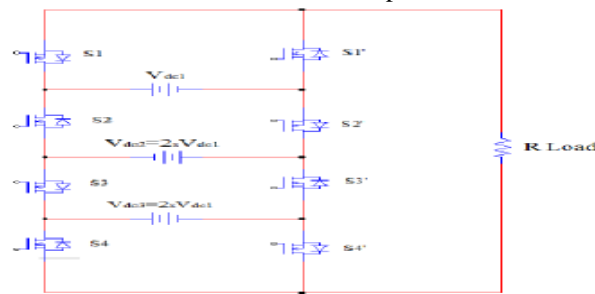


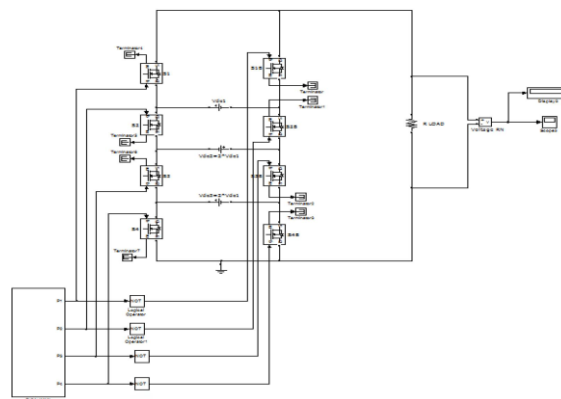Fig. Proposed configuration for single phase inverter operation



Fig.2. Simulation Circuit of the proposed inverter Configuration

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TABLE.2
SWITCHING STATES IN 11-LEVEL INVERTER

| Output Voltage | S1 | S2 | S3 | S4 | S1B | S2B | S3B | S4B |
|---|---|---|---|---|---|---|---|---|
| $+5V_{dc}$ | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| $+4 V_{dc}$ | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| $+3 V_{dc}$ | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| $+2 V_{dc}$ | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| $+ V_{dc}$ | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| $- V_{dc}$ | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| $-2 V_{dc}$ | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| $-3 V_{dc}$ | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| $-4 V_{dc}$ | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| $-5V_{dc}$ | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

Fig.3 shows the conducting switches at different operating states. +Vdc level voltage is obtained by turning on the switches Sl, S2B, S3B and S4B together. Similarly, all the DC output voltage levels are obtained as shown in T ABLE.2.
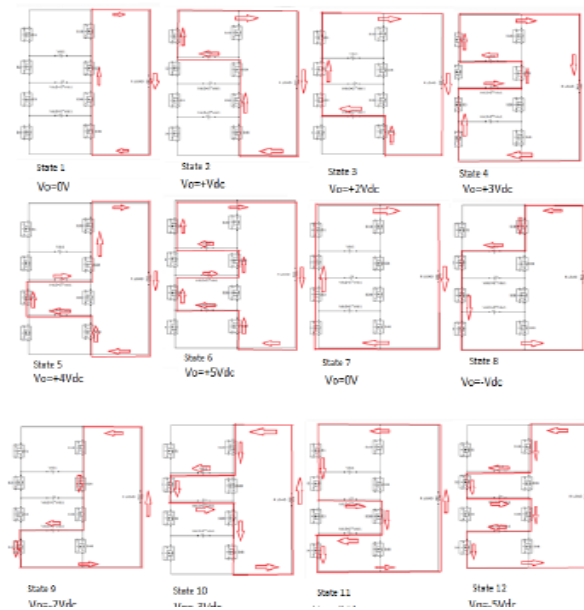


Fig.3. States corresponding to each Output voltage level

## III. MODULATION SCHEMES

To control the frequency and harmonics of the output voltage of the inverter, we must select the most appropriate PWM technique. The sinusoidal PWM (SPWM) method has been applied to the power switches, in which a reference sinusoidal wave of fundamental frequency is compared to high frequency carrier wave(s). The level, frequency or amplitude of the multiple carrier signals are varied based on the PWM technique. The modulation indices are kept same in all the methods for comparison. Amplitude modulation index is the ratio of the amplitude of the reference sine wave to the amplitude of the carrier waves. Frequency modulation index, is defmed as the ratio of the frequency of carrier wave to the frequency of the modulating wave. Amplitude modulation index rna and frequency modulation index mr are given by (1) and (2) respectively

$$m_a = A_m / A_c \qquad (1) \qquad m_f = f_c / f_m \qquad (2)$$

The PWM techniques discussed in this paper are InPhase Disposition (lPD) type level shift pulse width modulation (LS-PWM), Anti-Phase Disposition (APD) PWM, Carrier Overlap (CO) PWM and Variable

Frequency (VF) PWM. The amplitude modulation index rna is maintained at 0.9 and the frequency modulation index mr at 200. The RMS value of the fundamental component of the output voltage and the total harmonic distortion (THD) are observed by using simulation results. In all the PWM techniques, 'N' number of carrier signals are used to obtain 2N+ 1 voltage levels. A. In-Phase Disposition Level-Shift PWM (IPD-LSPWM) Method The carrier signals are level shifted in this PWM technique. They have the same amplitude of 1 V and a frequency of 10kHz. The level shifted carrier signals are compared with a diode bridge rectified reference sine wave which is at fundamental frequency, as illustrated in Fig.4. The different levels of the output wave is detected and decoded to produce the pulses required to trigger each switch in the inverter. In order to obtain a three phase inverter, the sine wave is phase shifted by 120°.
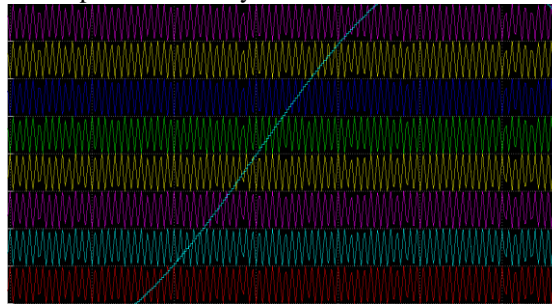


Fig.4. Reference Sine wave and Carrier waves for

## B. Anti-Phase Disposition Level-Shift PWM (APD-LSPWM) Method

Each carrier signal is out of phase with neighboring carrier signals by 180° and have the same amplitude and frequency. The carrier signals are compared with the reference sine wave (which is at fundamental frequency) to produce required gate pulses as shown in Fig.5.
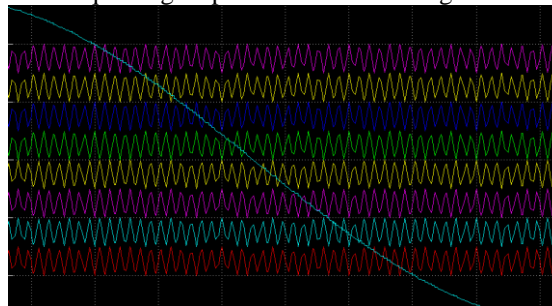


Fig.5. Reference Sine wave and Carrier waves for A PD-LSPWM at m a☐O.9 and m r200.

## C. Carrier Overlap PWM (CO-PWM) Method

This strategy utilizes level shifted carrier waves of the same frequency and amplitude. They are in phase with each other and also overlap each other. They are compared to a diode bridge rectified reference sine wave in Fig.6 in order to produce the gate pulses.
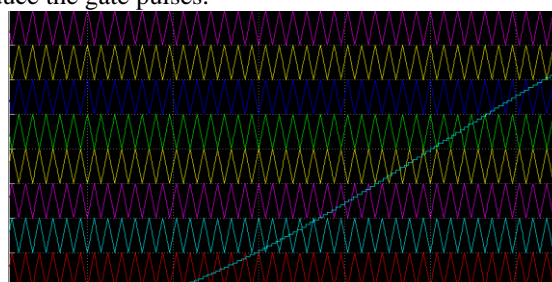


Fig.6. Reference Sine wave and Carrier waves Jor COPWM method at ma=O.9 and mJ=200.

## D. Variable Frequency PWM (VF-PWM) Method

In Fig.7, all the level-shifted carrier waves have the same amplitude. The lowermost carrier wave has very high frequency, 10kHz followed by 8kHz, 6kHz, 4kHz and the uppermost carrier signal has lowest

frequency, 2kHz. They are compared with the reference sine wave with fundamental frequency to produce required switching pulses.
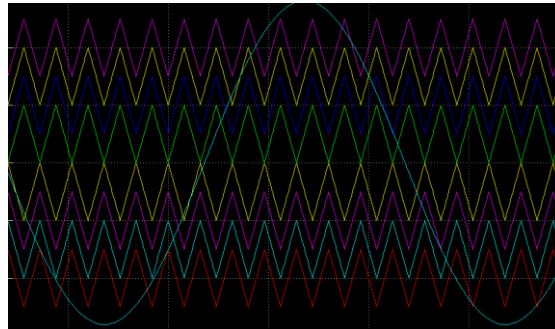


Fig.7. Reference Sine wave and Carrier waves Jor VF-PWM at ma=O.9

## IV SIMULATION RESULTS & DISCUSSION

Various PWM techniques are applied to the proposed three phase inverter topology at the same amplitude and frequency modulation indices using MATLAB/ Simulink. A comparative study has been made between the RMS values of fundamental value of the output voltage and the total harmonic distortion for a single phase using the Fast Fourier Transform (FFT) block. The circuit parameters used is:

$f_c = 10kHz; f_m = 50Hz; A_m = 4.5V; A_f = 5V.$

Star connected resistance load (R = 50Ω)    The three phase output voltage waveform obtained from IPD-LSPWM method is shown in Fig.8. It has significant 11 th, 17th, 21St, 25th, 27th and 29th harmonic values as given by its FFT analysis in Fig.9. The fundamental value of output voltage is higher and the THD is lesser in the IPD type LSPWM than the APD type. The carrier waves are in phase with each other in the IPD type, resulting in less complex circuitry
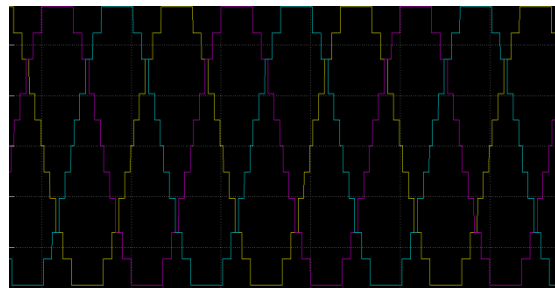


Fig.8. Output voltage waveforms for three phase 11 level inverter using IPDLSP WM technique.
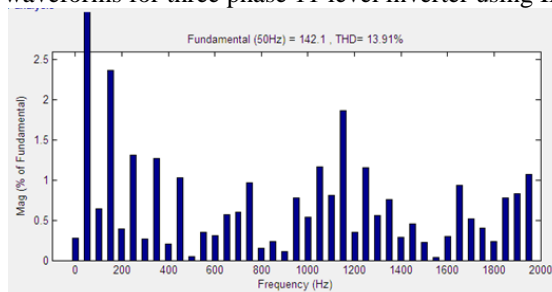


Fig.9. FFT Analysis of the harmonic spectrum for IPD-LSPWM technique

The output voltage and the FFT analysis for DLSPWM technique are shown in Fig.10 and 11 respectively. The 17th, 21st, 23rd, 25th, 27th ad 29th harmonics are   significant
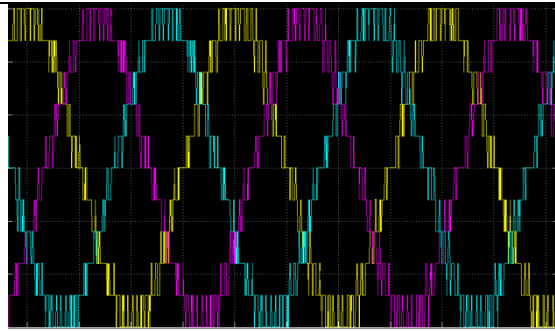
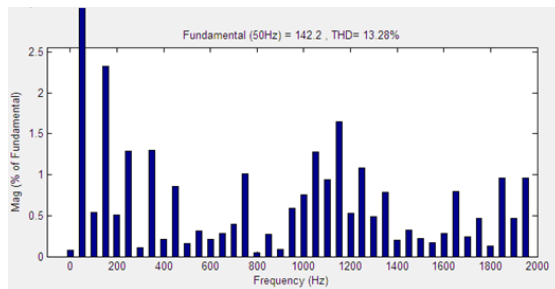Fig.10. *Output voltage waveform for three phase 11 level Inverter using APDLSPWM technique.*



Fig.11. *FFT Analysis of the harmonic spectrum for APD-LSPWM technique*

Fig.13 provides the FFT analysis of the output voltage of CO-PWM method is shown in Fig 12. The 3rd, 5th, 7th and 17th harmonics have higher energy. The output produced by CO-PWM has highest THD of 54.80% and lowest RMS value of fundamental output voltage of 127V among the four methods. This method produces pulses that overlap each other. Hence, the resultant voltage waveform has very high THD, which is not close to the sine wave. The carrier waves have larger amplitudes than other PWM techniques.
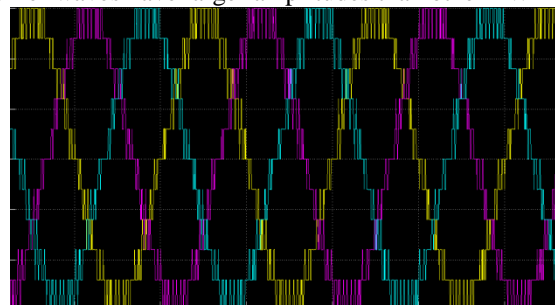


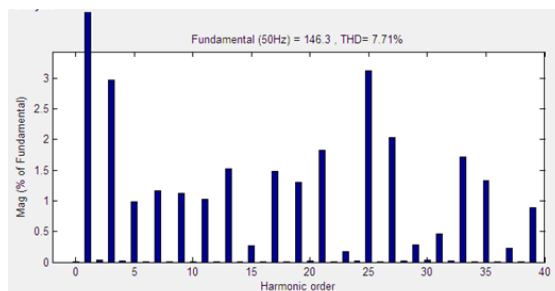Fig.12. *Output voltage waveform for three phase 11 level Inverter using CO-PWM technique.*



Fig.13. *FFT Analysis of the harmonic spectrum for CO-PWM technique*

The FFT of the inverter output voltage in Fig.14 from the VF-PWM method is demonstrated in Fig.15. The THD obtained through this method is only 12.51%. The spectrum has more 17th, 37th and 39th harmonic energy. Different carrier frequencies are used in this method, resulting in utilization of more analog components and large circuitry. The size and cost of the circuit can be reduced by opting for digital pulse generation, by using a suitable microcontroller kit.
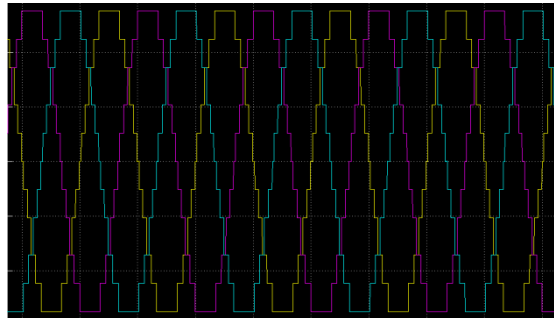
Fig.14. *Output voltage waveform for three phase 11 level Inverter using VFPWM technique.*
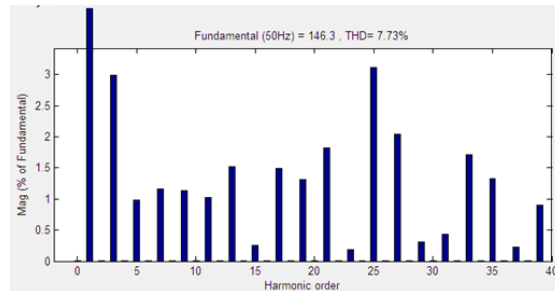


Fig.15. *FFT Analysis of the harmonic spectrum for VF-PWM technique*

The performance analysis of the three phase inverter based on the THD of the output voltage is given in Table.3. VF-PWM technique was found to be providing minimum harmonics in the output voltage among the four types.

TABLE.3
VRMS (FUNDAMENTAL) AND THD OF OUTPUT VOLTAGE FOR CHOSEN TOPOLOGY FOR DIFFERENT PWM TECHNIQUES

| SLNo. | PWM Technique | RMS Value of Fundamental of Output Voltage (in Volts) | THD (in %) |
|-------|---------------|-------------------------------------------------------|------------|
| 1 | IPD-LSPWM | 136.5 | 17.65 |
| 2 | APD-LSPWM | 135.9 | 17.76 |
| 3 | CO- PWM | 127 | 54.80 |
| 4 | VF- PWM | 134.1 | 12.51 |

**OUTPUT AFTER USING AN LC FILTER**

An L-C filter is connected at the output of the inverter to produce a sinusoidal waveform with reduced THD. The L and C values are designed to maintain the switching ripple current under the target value. The inductance value is thus given by:

$$L \geq \frac{R_{L-max}}{3\omega} \text{ for single phase} \qquad (3)$$

$$L \geq \frac{2*R_{L-max}}{p(p^2-1)\omega} \text{ for polyphase} \qquad (4)$$

(Where p=number of phases and w=21tf ).
The three phase inverter is connected to a star connected pure resistance load of son. The capacitance value of the filter is assumed to be 1 /IF.
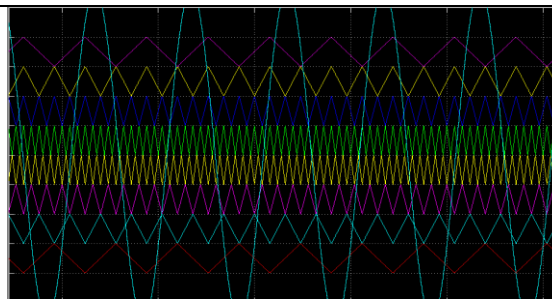
Fig.16. Sinusoidal output voltage waveform for three phase 11 level inverter using VF-PWM technique with series LC filter.

The signal obtained after the LC filter exhibits 1.77% THD. Fig.17 provides the details of the harmonics of the output AC voltage waveform in Fig.16.
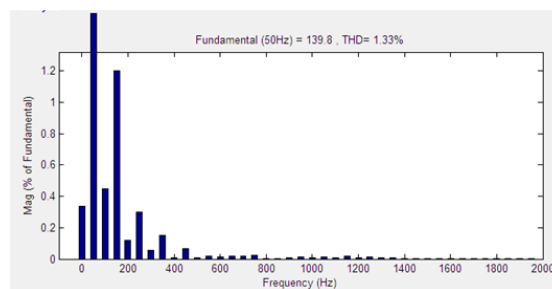


Fig.17. FFT Analysis of the harmonic spectrum for VF-P WM technique (with LC filter)

## VI. CONCLUSION

Three phase eleven level inverter topology with less number of switches is proposed and simulated. Various PWM methods are analyzed and compared. From the simulation results, it was found that VF-PWM provides minimum THD of 12.51 % in the inverter output voltage. This will be the best PWM technique for inverter switching because small inductance can be used in the LC filter placed in series to the inverter output to produce a rectified AC sine wave of low THD of 1.33%.

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