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UPQC for Power Quality improvement in DG integrated Smart Grid Network

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Abstract: A new proposal for the placement and integration of UPQC in DG connected microgrid/micro generation (μG) system has been presented here. DG converters (with storage), the load and shunt part of the UPQC will be placed at or after the PCC. The series part of the UPQC will be placed before the PCC and in series with the grid. DC link can be connected to the storage system also. Hence, it is termed UPQCμG. The advantages of the proposed UPQCμG over the normal UPQC are to compensate voltage interruptions in addition to voltage sags / swells, harmonic and reactive power compensation in the interconnected mode. The DG Converter with storage will supply the active power only and the shunt part of the UPQC will compensate the reactive and harmonic power of the load in the islanding mode. Therefore, the system can work both in interconnected and islanded mode. DG Converter does not require to be disconnected during the voltage disturbance. In all conditions, DG Converter will only provide the active power to the load and grid. Thus it will reduce the control complexity of the DG converter as well as improve the PQ of the network.

Index Terms: Unified Power Quality Compensator, Microgrid, Power Quality, Distributed Generation, Smart Grid

I. INTRODUCTION

As a part of the integration of the UPQC in a DG connected grid/μG system, research to date has been carried out on two techniques; i) (DG-UPQC)DC-linked and ii) (DG-UPQC)Separated. The pros and cons of these configurations are given below . The main problems for the configurations are i) the control complexity for active power transfer, ii) inability to provide harmonic and reactive power compensation during the islanded mode and iii) difficulty in the capacity enhancement in multi-level or multi-module mode. On the other hand, DG converter shall detect the unintentional islanding and cease to energize the islanded area within two seconds of the formation of an island . One of the reasons is that the controller of the grid-tie DG converter is designed to provide only the active power to the load and grid in the interconnected mode. For a seamless power transfer between the grid-connected operation and islanded mode, that is transfer between the current and voltage control modes of operation along with the robustness against the islanding detection and reconnection delays, research on hybrid control converter is underway . Clearly this will further increase the control complexity of the converter. However, the DG converter needs to be disconnected or to change its control strategy to work in the islanding mode after detecting the unintentional islanding. To extend the operational flexibility and to improve the power quality in grid connected μG systems, integration technique of UPQC have been proposed here. The μG system (with storage), the load and shunt part of the UPQC (APFsh) will be placed at or after the PCC. The series part of the UPQC (APFse) will be placed before the PCC and in series with the grid. DC link can be connected to the storage system also. Hence, it is termed UPQCμG. The UPQC current sensor, for reactive and harmonic power compensation, will measure only the load current. The main advantages of the proposed UPQCμG over the conventional UPQC are as follow.

- UPQCμG will compensate voltage interruptions in addition to voltage sags/swells, harmonic and reactive power compensation in the interconnected mode. Therefore, the DG converter can still be connected to the system during the voltage sag/interrupt condition. Thus it will extend the operational flexibility of the DG converters in the μG system.
- It will also compensate the reactive and harmonic (QH) power of the load in islanded mode.
- Due to the integration technique, the DG converter will then be more flexible to be islanded. Both in the current and voltage control modes, the μG system will provide only the active power to the load. Therefore, it can reduce the control complexity of the converter

II. WORKING PRINCIPLE

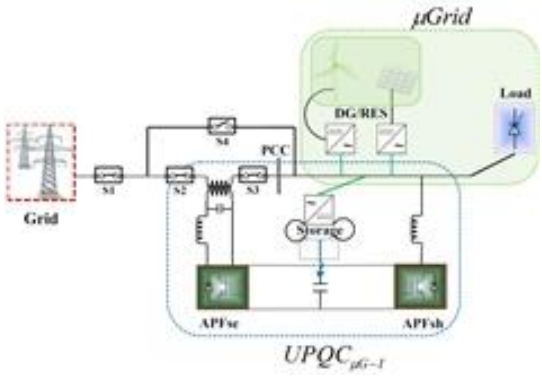
The integration technique of the proposed UPQCμG to a grid connected and DG integrated μG system is presented in Fig 1(a). The working principle during the interconnected and islanded mode for this configuration is shown in Fig 1(b, c).

A. Interconnected mode

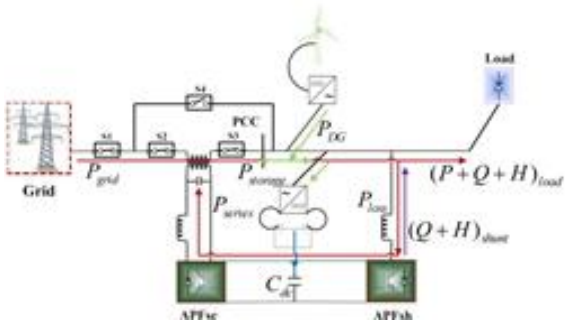
In this mode, as shown in Fig 1(b), the following will happen.

i. The DG source will deliver only the fundamental active power to the grid, storage and load.
ii. The APFsh will compensate the reactive and harmonic (QH) power of the non-linear load to keep the THD at the PCC within the IEEE standard limit.
iii. Voltage sag/swell/interruption can be compensated by the active power from the grid/storage through the APFse. DG

converter will not sense any kind of voltage disturbance at the PCC and hence will remain connected in any condition. iv. If the voltage interruption/black out occurs then UPQC will send a signal to the DG converter to be islanded



(a)



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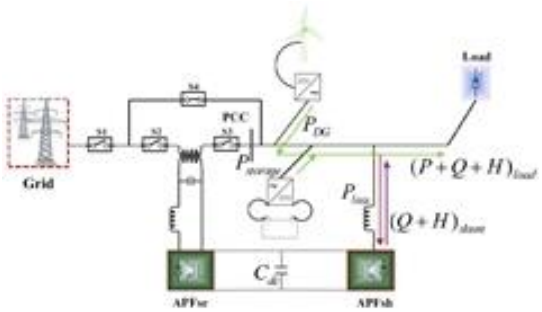


(c)

Fig 1: (a) Integration technique of the UPQCμG; (b) Working principle in interconnected and (c) islanded mode

B. Islanded mode

In this case, as shown in Fig 1(c), the following will occur.

i. The APFse will be disconnected during the grid failure and DG converter will remain connected and maintain the required voltage at PCC.

ii. The APFsh will still compensate the non-active power of the non-linear load to provide or maintain undistorted current at PCC for other linear loads (if any).

iii. Therefore, DG converter (with storage) will deliver only the active power and hence does not need to be disconnected from the system.

iv. The APFse will be reconnected once the grid power is available. From Fig 1, it is clear that the UPQCμG requires four switches. As the synchronization and reconnection control are part of the DG converter, after synchronization the converter is directly reconnected (through S4 and S1) to the grid and then sends an activation signal to UPQCμG to prepare for reconnection. After a suitable time, APFse of UPQCμG reconnects through S2 and S3 (by deactivated S4). A detail of the switching mechanism is discussed in the controller design section.

III. CONTROLLER DESIGN

The block diagram of the proposed UPQCμG Controller is shown in Fig 2. It has the same basic functionality as the UPQC controller except for the additional signal generation for islanding detection technique and reconnection capabilities. A communication channel between the proposed UPQCμG and the μG is also required for the detection of islanding and reconnection. This signal generation are based on the sag/swell/interrupt/supply failure conditions. This task is performed in Level 2 (secondary control) of the hierarchical control . Level 1 deals with the primary control of the series and shunt parts of the UPQC to perform their basic functions in the interconnected and the islanded mode. The overall integration technique and control strategy are to improve the power quality during interconnected and islanded modes. This involves detecting islanding and then ensuring that the DG converter remains connected and supplying active power to the load. This reduces the control complexity of the converter as well as the power failure possibility in the islanded mode. As the signal generation for Islanding detection (Sig-IsD) and Synchronization for Reconnection (Sig-Sync) are new in UPQC therefore, these have been described in details.

A. Sig-IsD

In order to ensure the reliable and safe transfer of electrical energy to the grid and load during the interconnected mode, all DG systems should comply with a series of standard requirements given in the international regulations . Considering the future trends towards the smart μG operation in connection with the distribution grid, the capability of (i) maintaining connection during grid fault condition, (ii) automatically detecting the islanded condition and (iii) reconnecting after the grid fault should be an important feature of the μG system.

In that case, the placement of APFse in the proposed integration method of the system will play an important role by extending the operational flexibility of the DG converter in the μG system. In addition to the islanding detection, changing the controlling strategy from current to voltage control may result in serious voltage deviations and it becomes severe when the islanding detection is delayed in the case of hierarchical control. Therefore seamless voltage transfer control between the grid-connected and isolated controlled modes is very important and it increases the control complexity of the μG converters.

In the case of power quality problems, it is reported that more than 95% of voltage sags can be compensated by injecting a voltage of up to 60% of the nominal voltage, with a maximum duration of 30 cycles . Therefore, based on the islanding detection requirement and sag/swell or other voltage disturbance compensation, a signal is generated for the islanding detection (Sig-IsD) in the proposed $UPQC_{\mu G}$ to transfer it to the DG converter. As the APF_{se} takes the responsibility for compensating voltage sag/swell/unbalance disturbances (depending on the controller), IsD algorithm in DC converter can be quite flexible and simple.

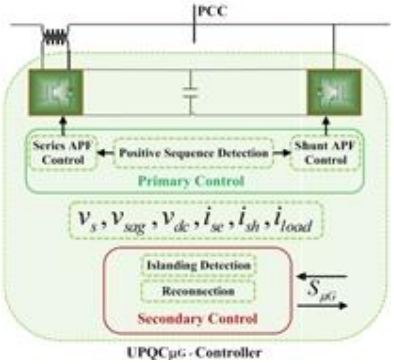


Fig 2: Block diagram of proposed UPQCμG Controller

Fig 3 shows the algorithm (with an example) that has been used to detect the islanding condition to operate the UPQCμG in the islanded mode. The voltage at PCC is taken here as the reference and it is always in phase with the source and the DG converter, the difference between the Vpcc-ref (pu) is . This error is then compared with the pre-set values (0.1 to 0.9) and a waiting period (user defined n number of cycles) is used to determine the sag/interrupt/islanding condition. In this example, (i) if Verror is less than or equal to 0.6, then 60% sag will be compensated for up to 50 cycles; (ii) if Verror is in between 0.6 to 0.9, then compensation will be for 30 cycles; (iii) otherwise (if Verror>0.9) it will be interrupt/black out for islanding after 1 cycle.

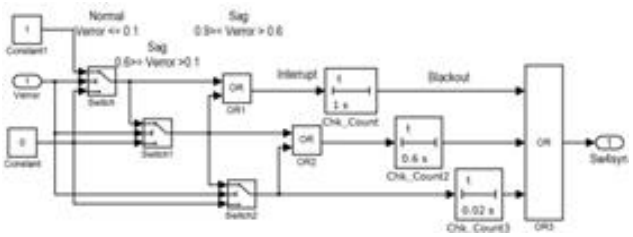
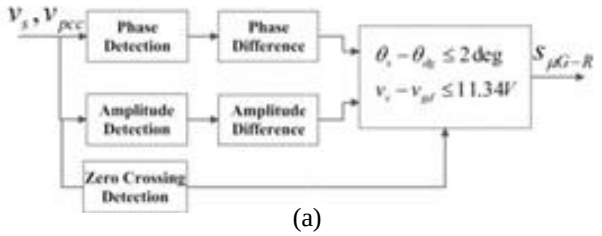


Fig 3: Signal generation for Islanding detection (Sig-IsD) method in simulink

This signal generation method is simple and can be adjusted for any time length and Verror condition. Thus the flexibility of time and control for compensating the sag can be achieved before islanding. As the seamless voltage transfer from grid connected to isolated mode is one of the critical tasks in transition period, the transfer will be completed at the zero crossing position of the APFse. Therefore, no voltage fluctuation or abrupt conditions will occur.

B. Sig-SynRec

Once the grid system is restored, the μG may be reconnected to the main grid and return to its pre-disturbance condition. A smooth reconnection can be achieved when the difference between the voltage magnitude, phase and frequency of the two buses are minimized or close to zero. In the case of the UPQCμG, the synchronization for reconnection is done by the DG converter. Once the voltage magnitude, phase angle and frequency differences are within the pre-defined range or are close to zero, then reconnection is made through S4 and S1 as shown in Fig 1. The μG control system then sends a signal SμG-R to the UPQCμG. The APFse is then activated and switches S2 and S3 are reconnected to the system by deactivating S4. This switching transition is controlled and performed at a zero crossing condition of Vs. As an example, Fig 4(a) shows a simple synchronization method for reconnection and SμG-R is the signal generated by the DG converter. This signal is activated when the phase difference between the utility (Vs) and PCC are within 2 deg in phase and corresponding voltage amplitude difference is within 11.24V. These are observed at a zero crossing of ☼ 0. Fig 4(b) shows the reconnection method of APFse for the UPQCμG. The activated SμG-R signal is taken from the μG and passed through a S-R Flip Flop to generate the active signal (Swsesyn) for APFse at the Vs zero crossing condition. This Swsesyn signal is then XOR to the Sw4syn (as shown in Fig 3) to generate the real activation signal for the APFse.



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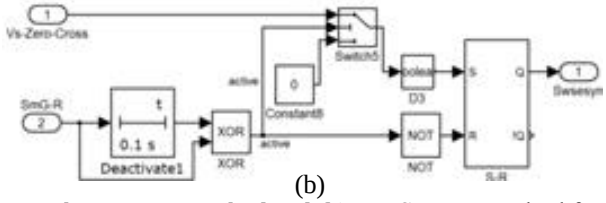


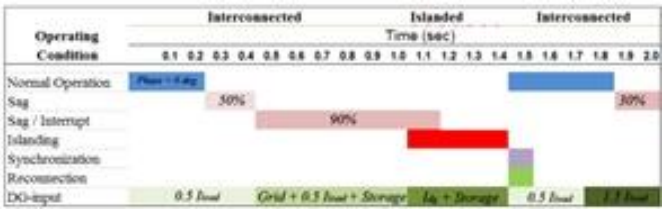
(b)

Fig 4: (a) Synchronization method and (b) Sig-SynRec method for UPQCμG

IV. SIMULATION STUDY

A 3-phase, 3-wire active distribution network (230VL-N) with the proposed UPQCμG and μG, as shown in Fig 1, has been developed in the MATLAB environment. The system specifications are as follow; UPQCμG (capability: 100% sag and 100Amax harmonic current compensation) and the μG (Load: 200Amax with harmonic 100Amax; DG: 0.5 to 1.5 times of load fundamentals). Details of the performance with the simulation results are given below. All the simulations have been performed for up to 2 sec. Table 1 shows the timeline for the respective operating conditions.

TABLE 1
TIMELINE OF THE OPERATING CONDITIONS



Based on the integration method and signal generation for islanding detection and the reconnection method, Fig 5(a) shows the switch positions (0 for open and 1 for close) during the operation from 0 to 2 sec where both the interconnected and islanded modes are observed. The performance of the proposed UPQCμG for voltage sag compensation is shown in Fig 5(b) and harmonic current compensation is shown in Fig 5(c) based on the Table 1. Performance during the reverse current flow due to the high penetration of DG is also shown by the red circle in Fig 5(c). Details of the performance at different conditions are discussed below. Generally waveforms are shown for phase A only.

A. Interconnected Mode

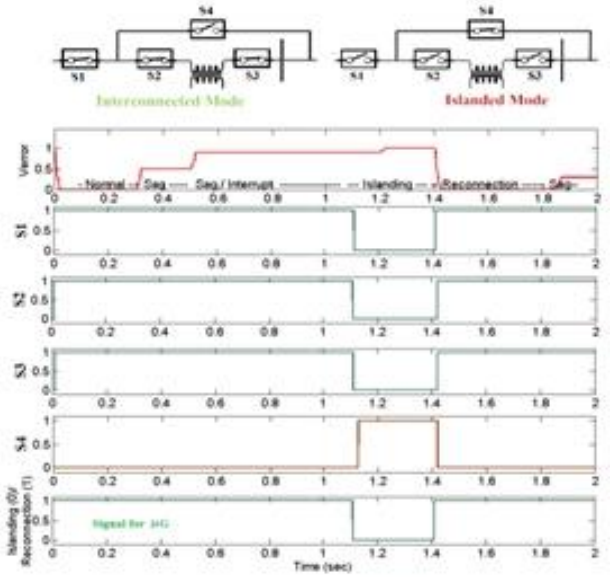
Depending on the power availability, the DG source can supply power to the load and grid, and therefore by- directional power flow can occur. Hence, the performance of the proposed UPQC should be observed in both cases. For a better understanding, according to the direction of power flow, operation in the interconnected mode can be divided into two parts: (1) forward-flow mode and (2) reverse-flow mode.

a. Forward-flow mode

In this case, the available DG power is less than the required load demand. Therefore, the utility supplies rest of the power to the load which is not met by the DG supply. Fig 6 shows the performance of the APFsh in compensating the reactive and harmonic current generated by the load. As is mentioned in the timeline table, the DG unit supplies 0.5□□□□□□ (half of load fundamental in current control mode) during this time frame. Therefore the remainder of the current is supplied by the utility grid and storage. During a 90% sag condition, the total power for the load demand is still met by the μG system (as shown in Fig 5) and the utility where the storage system provides the power for sag compensation through the DC link.

b. Reverse-flow mode

When the available DG power becomes higher than the required load demand, the extra energy is transferred to the grid and storage and this is termed the reverse-flow mode. At this stage, the grid current becomes out of phase with the voltage at PCC. Fig 7 shows the performance of the system when DG current becomes 1.5□□□□□□ at 1.75 sec and a 30% sag is also applied at 1.85 sec.



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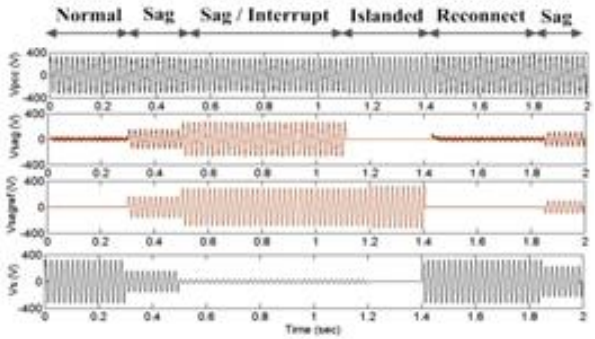

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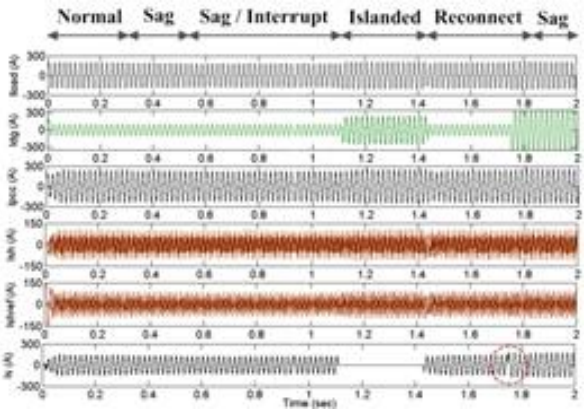


(c)

Fig 5: (a) Switching positions during the operation; (b) voltage and (c) current waveforms at difference conditions and positions in the network.

B. **Islanded Mode**

According to the Sig-IsD method, the APFse compensates the sag for up to 0.6 sec (30 cycles) and then the system goes into islanded mode. A utility disconnection is applied at 1.11 sec just after completing the 30 cycle count and then detecting the zero crossing of ๐0□□◌̂□□□ where S1, S2 and S3 are opened. This is depicted

in Fig 8. At disconnection, the µG operates in islanded mode. At this stage, if the available DG power is lower than the load demand, the required power is supplied by the storage. If the DG power is higher than the load, then the additional power goes to the storage. The APFsh still performs the compensation of non-active power. Therefore, DG converter does not need to be disconnected or change the control strategy (supply only the fundamental active power) to supply power to the load.

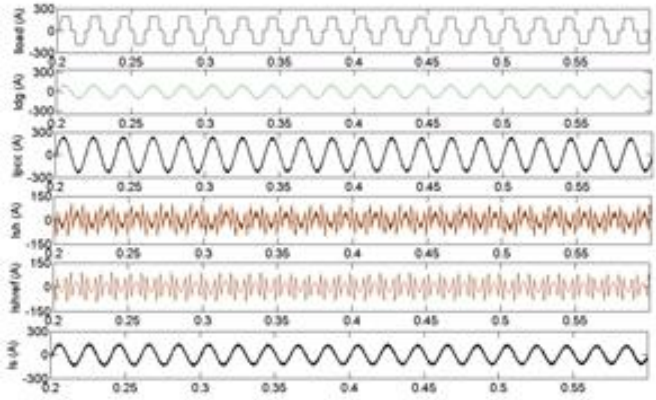


Fig 6: Performance of APFsh in interconnected and forward flow mode

Fig 8 shows the performance of the proposed UPQCµG during 1.0 to 1.2 sec where the islanding is detected just immediately after 1.1 sec at zero crossing detection. The islanding mode is observed between 1.11 and 1.405 sec. During this period the APFse is disconnected, as shown in Fig 8(b) where Vsag = 0, utility current become zero, as shown in Fig 8(c). The APFsh continues to operate, as shown in Fig 8(c), and the load demand is met by the DG with the storage unit.

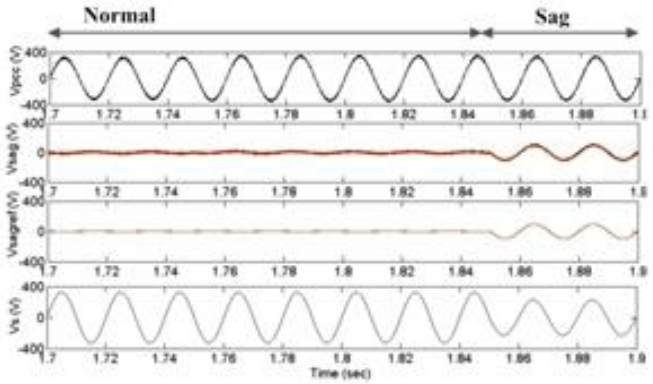
C. Reconnection

Fig 9(a) shows the different signals for the reconnection process based on the Sig-SynRec method showed in Fig 4. To check the performance of the reconnection process for the worst condition, the utility grid (Vs) is powered on at 1.405 sec where the magnitude is at a maximum, as shown by the red circle in Fig 9(b). Zero crossing detection is also shown. The DG unit sends a reconnection signal, to the UPQCµG unit. Based on the logic given in Fig 11, the actual switch S1 is activated at 1.43 sec and the Vsag starts operation, as shown by the red circle in Fig 9(b). S2 and S3 are activated after the synchronization by the DG unit. S4 is disconnected simultaneously at 1.44 sec. This simple algorithm with a combined logic gate ensures the utility connects with the µG smoothly after the utility system is restored.

Fig 9(b) shows that the APFse unit is immediately reactivated when the grid voltage is available at 1.405 sec but it starts operation when the S2 and S3 switches are closed at 1.43 sec. It is expected that, according to the smooth reclosing condition, no power flow will occur at the point of reclosing. The switching is carried out successfully within the limiting condition as shown in Fig 9(c). The circle at 1.43 sec for Idg and Is in Fig 9(c) indicates the smooth transition from islanded to interconnected mode. DG converter also changes its control from voltage to current control mode but only transfers the active fundamental current. The performance of the APFsh is also uninterrupted during the transition period.

D. Power Flow

The power flow diagram is shown in Fig 10 for the complete simulation time where the green line represent the active power (P) and red line (dash) for reactive and harmonic power (QH). This also validates the operation and performance of the APFse and APFsh part of the proposed UPQCµG along with the islanding detection and reconnection.



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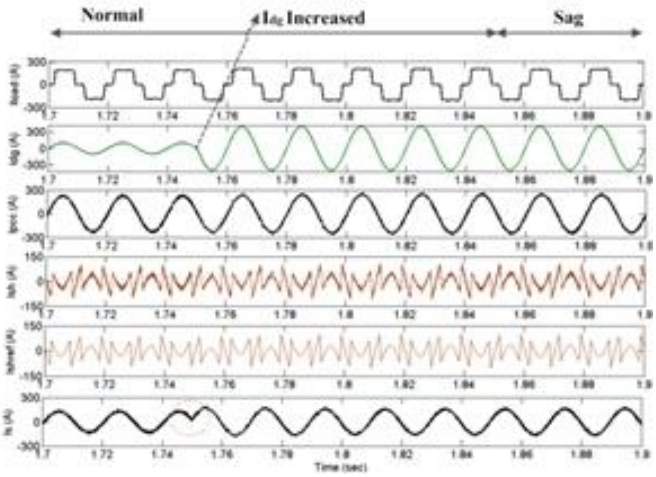
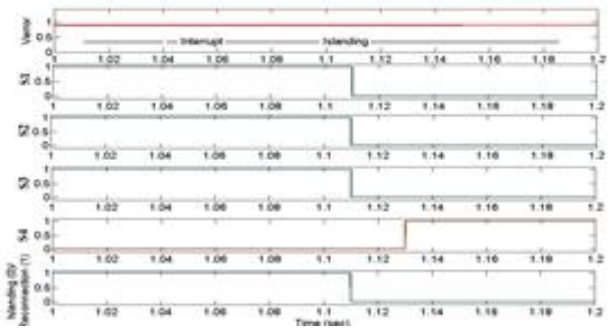


(b)

Fig 7: Performance; a) APFse; b) APFsh; interconnected and reverse flow

V. CONCLUSION

This paper describes a new placement and integration technique of the UPQCμG in the grid connected μG condition. The simulation has been performed in MATLAB. The results show that the proposed system can compensate the voltage disturbance at the PCC, the reactive and harmonic current compensation of the load that could inject at the PCC during the interconnected mode. Performance of the UPQCμG is also observed in bi-directional power flow condition. During the islanded mode, the DG converter also only supplies the active power to the load and the shunt APF performs the reactive and harmonic power compensation. Therefore, the grid-tie DG converter does not need to be disconnected or change its control strategy to keep the μG operating during the islanding detection and operation in islanded mode.



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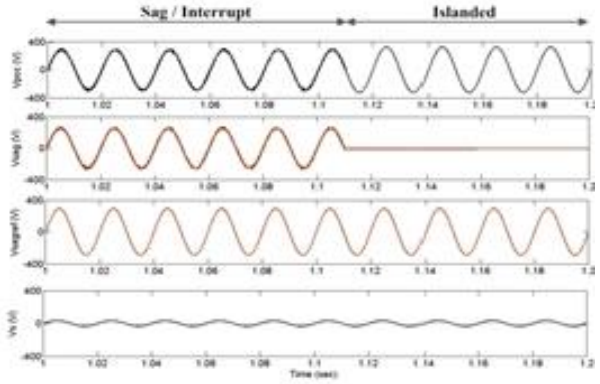

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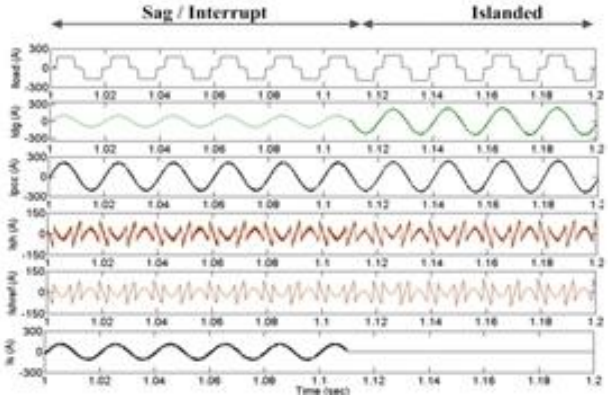
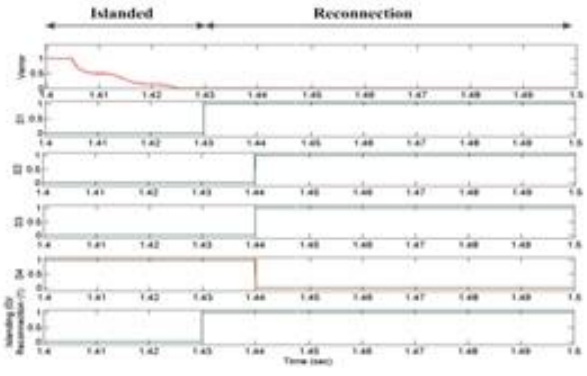


(c)

Fig 8: Performance -(a) switching, b) APFse, c) APFsh during islanded mode



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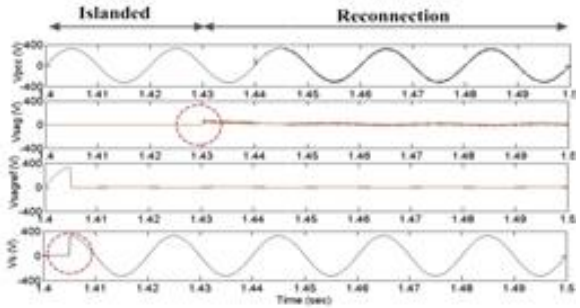

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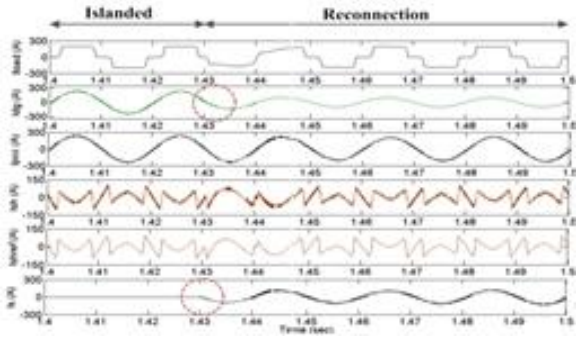

(c)
Fig 9: Reconnection -(a) switching, (b) APFse; (c) APFsh

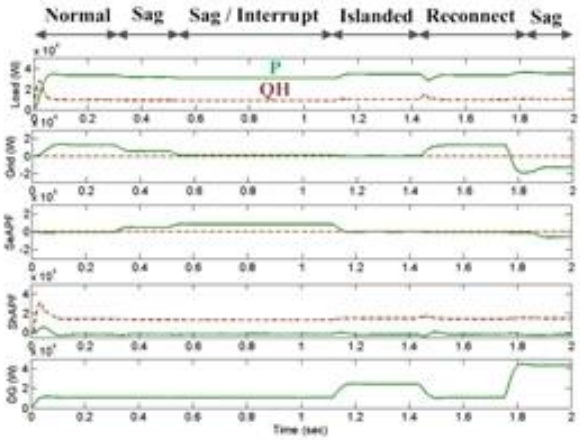

Fig 10: Power flow during the simulation time

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