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Simulation of D-STATCOM for Power Quality Improvement With Fuzzy Based Phase Locked Loop Control Strategy

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Abstract: Power quality in distribution systems affects all the connected electrical and electronics equipments. It is a measure of deviations in voltage, current, frequency of a particular system and associated components. DSTATCOM is one of the important devices for improving power quality. The cascade multilevel inverter based DSTATCOM has been widely used in various DSTATCOM prototypes and projects due to its advantages such as low loss, high efficiency, little harmonic content in output voltage, easy modularization, and so on. However, this kind of DSTATCOM structure contains controlling problems, which may lead to abnormal running of DSTATCOM, especially in the transient process running of DSTATCOM. In order to solve the controlling problem, a control algorithm based on enhanced phase-locked loop (EPLL) for distribution static compensator (DSTATCOM) to compensate reactive power, to provide load balancing, to eliminate harmonics, to correct power factor, and to regulate point of common coupling (PCC) voltages under linear and nonlinear loads. In this approach, an extraction of fundamental active and reactive power components of load currents for the estimation of source currents includes a signal-processing algorithm based on the EPLL scheme. The proposed control algorithm is implemented using a digital signal processor**.** Test results on a developed DSTATCOM are presented to validate the proposed control algorithm for compensation of reactive power, load balancing, harmonic elimination, power factor correction and zero voltage regulation at PCC.

Keywords: DSTATCOM, enhanced phase locked loop(EPLL),point of common coupling(PCC),cascade multi inverter.

I.INTRODUCTION

In recent years Electrical Power Quality had obtained more attention in power engineering. In present day's power distribution systems is suffering from severe power quality problems. These power quality problems include high reactive power burden, harmonics currents, load unbalance, excessive neutral current etc. The measure of power quality depends upon the needs of the equipment that is being supplied. What is good power quality for an electric motor may not be good enough for a personal computer. Usually the term power quality refers to maintaining a sinusoidal waveform of bus voltages at rated voltage and frequency. A DSTATCOM is a device which is used in an AC distribution system where, harmonic current mitigation, reactive current compensation and load balancing are necessary. The building block of a DSTATCOM is a voltage source converter (VSC) consisting of self commutating semiconductor valves and a capacitor on the DC bus. The device is shunt connected to the power distribution network through a coupling inductance that is usually realized by the transformer leakage reactance. In general, the DSTATCOM can provide power factor correction, harmonics compensation and load balancing. The major advantages of DSTATCOM compared with a conventional static VAR compensator (SVC) include the ability to generate the rated current at virtually any network voltage, better dynamic response and the use of a relatively small capacitor on the DC bus.

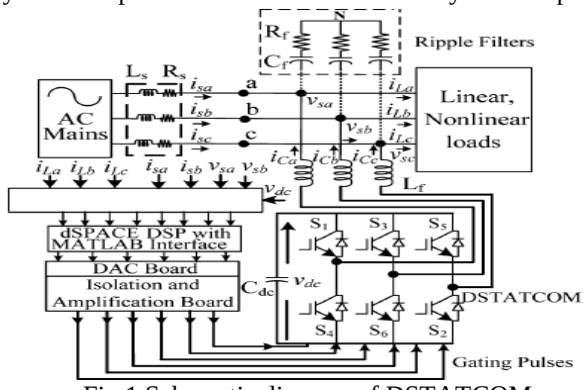


Fig.1 Schematic diagram of DSTATCOM

A DSTATCOM is a device which is used in an AC distribution system where, harmonic current mitigation, reactive current compensation and load balancing are necessary. The building block of a DSTATCOM is a voltage source converter (VSC) consisting of self commutating semiconductor valves and a capacitor on the DC bus. The device is shunt connected to the power distribution network through a coupling inductance that is usually realized by the transformer leakage reactance. In general, the DSTATCOM can provide power factor correction, harmonics compensation and load balancing. The major advantages of DSTATCOM compared with a conventional static VAR compensator (SVC) include the ability to generate the rated current at virtually any network voltage, better dynamic response and the use of a relatively small capacitor on the DC bus.

II. DESIGN OF MULTILEVEL BASED DSTATCOM

2.1 Principle of DSTATCOM

A D-STATCOM (Distribution Static Compensator), which is schematically depicted in Figure- I, consists of a two level Voltage Source Converter (VSC), a dc energy storage device, a coupling transformer connected in shunt to the distribution network through a coupling transformer. The VSC converts the dc voltage across the storage device into a set of three-phase ac output voltages. These voltages are in phase and coupled with the ac system through the reactance of the coupling transformer. Suitable adjustment of the phase and magnitude of the D-STATCOM output voltages allows effective control of active and reactive power exchanges between the DSTATCOM and the ac system. Such configuration allows the device to absorb or generate controllable active and reactive power. The VSC connected in shunt with the ac system provides a multifunctional topology which can be used for up to three quite distinct purposes

i. Voltage regulation and compensation of reactive power;
ii. Correction of power factor
iii. Elimination of current harmonics.

Here, such device is employed to provide continuous voltage regulation using an indirectly controlled converter. As shown in Figure-l the shunt injected current Ish corrects the voltage sag by adjusting the voltage drop across the system impedance Zth. The value of Ish can be controlled by adjusting the output voltage of the converter. It may be mentioned that the effectiveness of the DSTATCOM in correcting voltage sag depends on the value of Zth or fault level of the load bus. When the shunt injected current Ish is kept in quadrature with V L, the desired voltage correction can be achieved without injecting any active power into the system. On the other hand, when the value of Ish is minimized, the same voltage correction can be achieved with minimum apparent power injection into the system. It may be mentioned that the effectiveness of the DSTATCOM in correcting voltage sag depends on the value of Zth or fault level of the load bus. When the shunt injected current Ish is kept in quadrature with V L, the desired voltage correction can be achieved without injecting any active power into the system. On the other hand, when the value of Ish is minimized, the same voltage correction can be achieved with minimum apparent power injection into the system.

2.2 Control for Reactive Power Compensation

The aim of the control scheme is to maintain constant voltage magnitude at the point where a sensitive load under system disturbances is connected. The control system only measures the rms voltage at the load point, i.e., no reactive power measurements are required. The VSC switching strategy is based on a sinusoidal PWM technique which offers simplicity and good response. Since custom power is a relatively low-power application, PWM methods offer a more flexible option than the fundamental frequency switching methods favored in FACTS applications. Apart from this, high switching frequencies can be used to improve on the efficiency of the converter, without incurring significant switching losses.

Fig.2 PI Control for reactive power compensation

The controller input is an error signal obtained from the reference voltage and the rms terminal voltage measured. Such error is processed by a PI controller; the output is the angle 0, which is provided to the PWM signal generator. It is important to note that in this case, of indirectly controlled converter, there is active and reactive power exchange with the network simultaneously. The PI controller processes the error signal and generates the required angle to drive the error to zero, i.e. the load rms voltage is brought back to the reference voltage.

III. DSTATCOM AND SYSTEM CONFIGURATION

The DSTATCOM consists of a voltage source converter (VSC) based on self commutating semiconductor valves and a capacitor on the dc bus. This compensating device is connected at point of common coupling (PCC) through interfacing inductances. In general, the functions of DSTATCOM are reactive power compensation, harmonics elimination, along with load balancing in the distribution system in PFC and ZVR modes of operation. Fig. 1 shows a schematic diagram of a DSTATCOM connected to a three phase ac mains having a source impedance feeding variety of three phase loads. Interfacing inductors are used at ac side of the VSC for reducing ripple in compensating currents. A series connected capacitor and a resistor represent the ripple filter installed at PCC in parallel with the loads and the DSTATCOM to filter the high frequency switching noise of the voltages at PCC. The compensating currents are injected by DSTATCOM to cancel harmonics/reactive power components of load currents.

IV. CONTROL ALGORITHM OF DSTATCOM

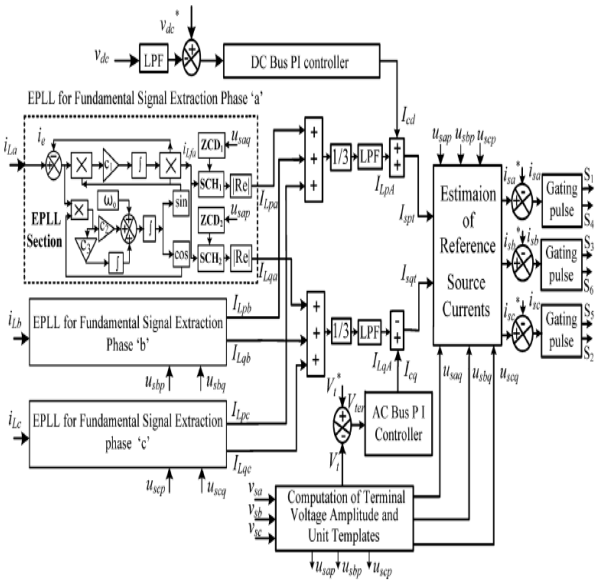


Fig. 3 Generation of reference source currents using the EPLL-based control algorithm

Fig. 3 shows a block diagram of proposed control algorithm based on EPLL scheme for extraction of reference source currents. Basic equations for estimation of different control signals of control algorithm are given as.

4.1 Estimation of In- Phase and Quadrature Unit Voltage Templates

Three phase sensed PCC voltages may consist of harmonics and negative sequence components. These PCC voltages are processed through band pass filters (BPFs) to filter noise and harmonics. These filtered PCC voltages may also be unbalanced. The individual amplitude of each of these three phase voltages are estimated through squaring them and then processed through low passed filters (LPFs) as follows:

$$V'_{ta} = \sqrt{[2(\frac{v_{sa}^2}{2})]} \quad \text{……..(1)} \qquad V'_{tb} = \sqrt{[2(\frac{v_{sb}^2}{2})]} \quad \text{……..(2)} \qquad V'_{tc} = \sqrt{[2(\frac{v_{sc}^2}{2})]} \quad \text{……..(3)}$$

After processing, these voltages (, and) through LPFs, these are constant valued amplitudes represented and for phases a, b, and c. In phase unit templates of PCC voltages are estimated as:

$$u_{sap} = \frac{v_{sa}}{V_{ta}} \quad \text{…….(4)} \qquad u_{sbp} = \frac{v_{sb}}{V_{tb}} \quad \text{……..(5)} \qquad u_{scp} = \frac{v_{sc}}{V_{tc}} \quad \text{……(6)}$$

Moreover, the quadrature unit templates are estimated as:

$$u_{saq} = \frac{(-u_{sbp} + u_{scp})}{\sqrt{3}} \quad \text{…….(7)} \qquad u_{sbq} = \frac{(3u_{sap} + u_{sbp} - u_{scp})}{2\sqrt{3}} \quad \text{……(8)}$$

$$u_{scq} = \frac{(-3u_{sap} + u_{sbp} - u_{scp})}{2\sqrt{3}} \quad \text{…….(9)}$$

The amplitude of PCC voltages v1 is estimated as:

$$v_t' = \sqrt{\frac{2(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)}{3}} \quad \text{……..(10)}$$

This amplitude may have ripples because of fundamental negative sequence voltage present in PCC voltages. This is processed through LPF to achieve amplitude of fundamental positive-sequence PCC voltages and it is represented as for the control of PCC voltages.

4.2 Estimation of Fundamental Active and Reactive Power Components of Load Currents

The fundamental active and reactive power components of load currents are estimated by using proposed control algorithm based on EPLL scheme in each phase. EPLL used in phase 'a' receives the input signal as the load current. Difference between and is the total distortion in the applied signal. It is denoted as . The selection process of EPLL internal parameters are described and it is shown that parameters, and control the steady state and transient behavior of EPLL. In this application, the values of, and are used as 17, 10, and 1, respectively, to estimate the fundamental load current signals. Similarly, other phases fundamental signals are extracted. The fundamental component of phase 'a' load current is in phase with the input signal and it moves with certain phase difference with the reference in-phase template. Therefore, to extract the amplitude of the fundamental active power component of load current in phase of the respective input PCC voltage, a zero crossing detector is used on quadrature template , which is shifted 90 from. Extracted fundamental load current is considered as an input to sample and hold block and output of is used as trigger pulses to this block. The output signal of the sample and hold block is considered as an amplitude of phase "a" fundamental active power component of load current. Similarly, other phase fundamental active power component of load currents (and) are also extracted. To extract fundamental reactive power component of load current of phase 'a', another zero crossing detector is used on in-phase template . Extracted fundamental load current is fed to second sample and hold block as an input and output of as a trigger pulse. The output signal of sample and hold block is taken as amplitude of phase 'a' reactive power component of load current. Similarly, phase "b" and "c" fundamental reactive power component of load currents and are also estimated.

4.3 Estimation of Average Amplitude of Active and Reactive Power Components of Load Currents

The average amplitude of fundamental active and reactive powers components of the three phase load currents are estimated using the amplitude of active and reactive power components of load currents. An average value of amplitudes is estimated for load balancing and to be used in the extraction of three phase reference source current as :

$$I_{LpA} = \frac{I_{Lpa} + I_{Lpb} + I_{Lpc}}{3} \quad \text{……..(11)} \qquad I_{LqA} = \frac{I_{Lqa} + I_{Lqb} + I_{Lqc}}{3}. \quad \text{……..(12)}$$

4.4. Estimation of Amplitude of Active Power Component of Reference Source Currents

To estimate another component of the reference active power component of source currents, the reference dc bus voltage is compared with sensed dc bus voltage of DSTATCOM. The dc bus voltage is regulated through PI (proportional-integral) controller which is required to maintain dc bus voltage. It is represented as . The amplitude of active power component of the reference source current is estimated as the addition of required active power component of current for the self supporting dc bus of the DSTATCOM and average magnitude of active power components of load currents as:

$$I_{spt} = I_{cd} + I_{LpA} \quad \text{…….(13)}$$

4.5. Estimation of Amplitude of Reactive Power Component of Reference Source Currents

The amplitude of another component of reactive power component of the reference source current is calculated using a voltage PI controller over the amplitude of the PCC voltage and its reference value. The voltage error of ac voltage at the th sampling instant is given as:

$$V_{ter}(r) = V_t^*(r) - V_t(r). \quad \text{…….(14)} \qquad I_{cq}(r) = I_{cq}(r-1) + k_{pt}\{V_{ter}(r) - V_{ter}(r-1)\} + k_{it}V_{ter}(r) \quad \text{……..(15)}$$

where is a part of the reactive power component of source current and it is named , and are the proportional and integral gain constants of the PCC voltage PI controller. The amplitude of reactive power component of the reference source current is estimated as the difference of output of the voltage PI controller and the average of reactive power component of load currents as:

$$I_{sqt} = I_{cq} - I_{LqA} \quad \text{……..(16)}$$

This component is required for the extraction of reference reactive power components of source currents. It is used for voltage regulation along with load balancing and harmonics elimination in addition to the reference active power components of source currents. However, for power-factor correction along with harmonic elimination and load balancing, amplitude of reference reactive power component of source currents is set to zero and in this condition and reference active power component of source currents are considered as total reference source currents. At a time, only one operating mode of DSTATCOM is possible out of PFC or ZVR.

V.SIMULATION RESULTS

Case-1 various intermediate signals of the proposed control algorithm of DSTATCOM

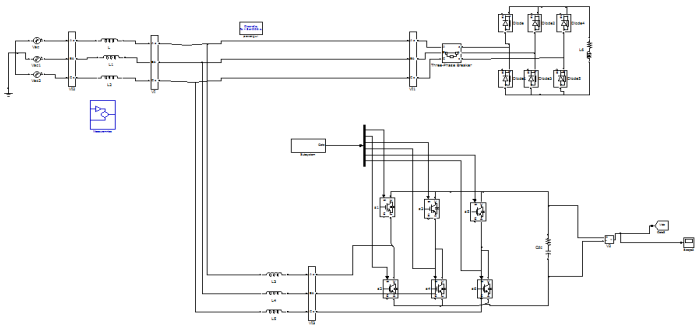


Fig.4 shows the Matlab/simulink model of proposed converter

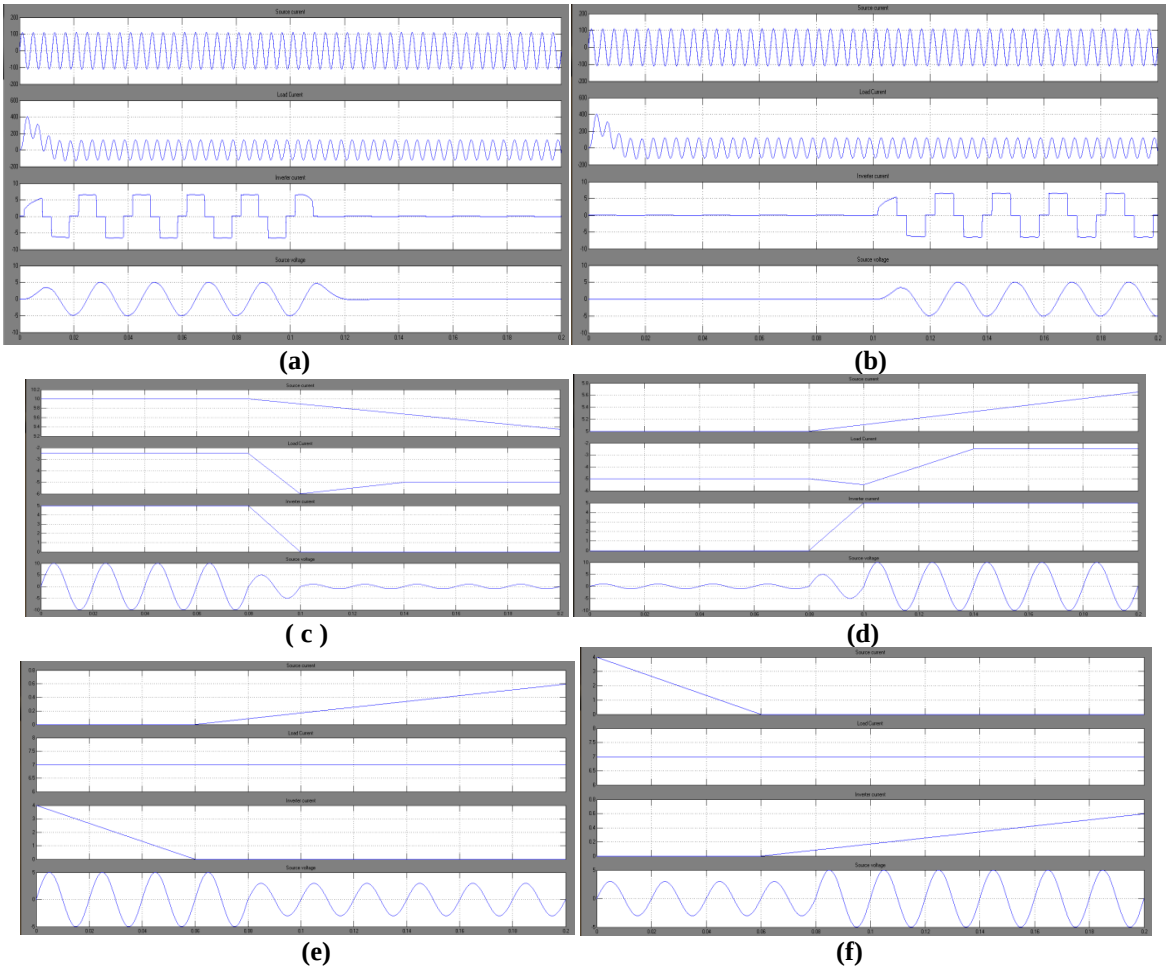
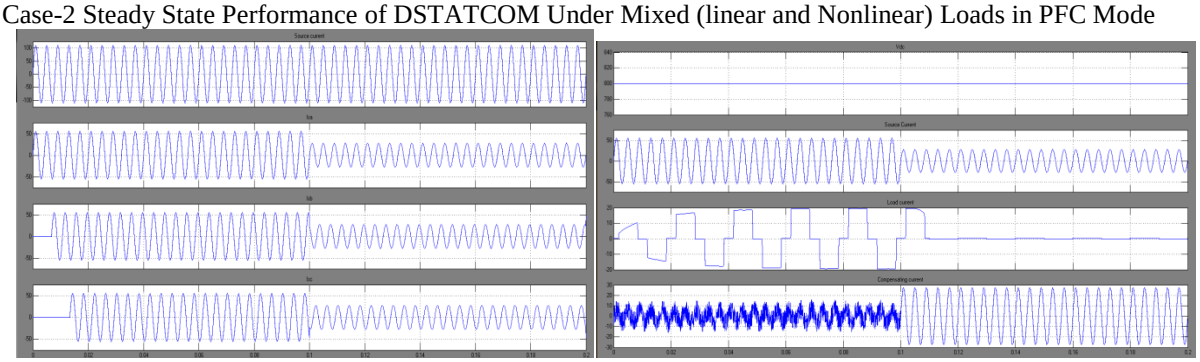


Fig. 5 (a)–(f) Various intermediate signals of the control algorithm at load removal and load injection

Case-2 Steady State Performance of DSTATCOM Under Mixed (linear and Nonlinear) Loads in PFC Mode



(a) **(b)**

Fig.6 Dynamic performance of DSTATCOM during unbalanced nonlinear loads (a) isa, isb, isc with Vab (b) Variation of isa, ila,ica, with vdc

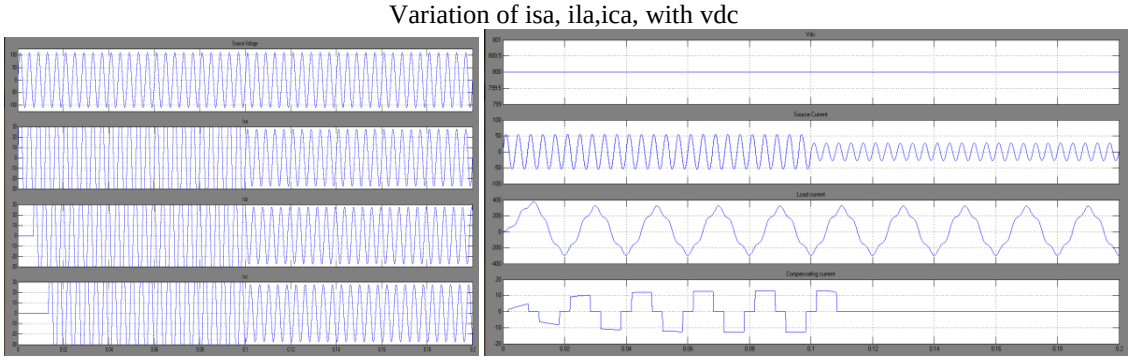
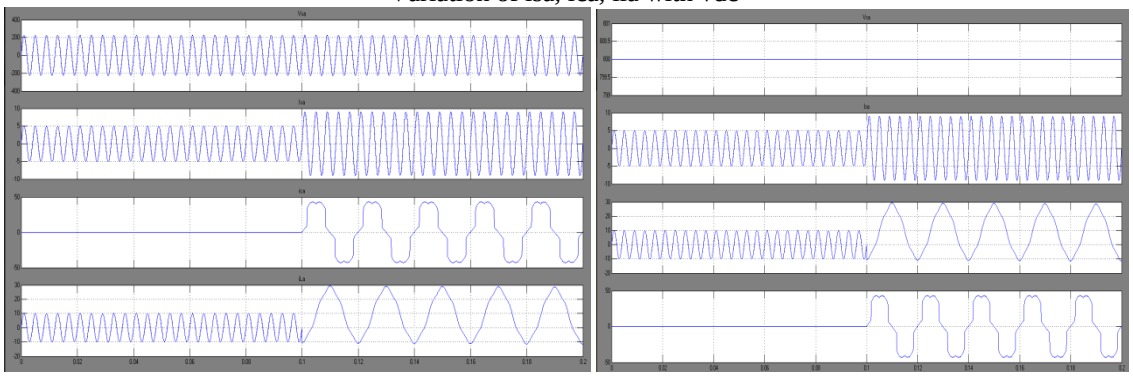
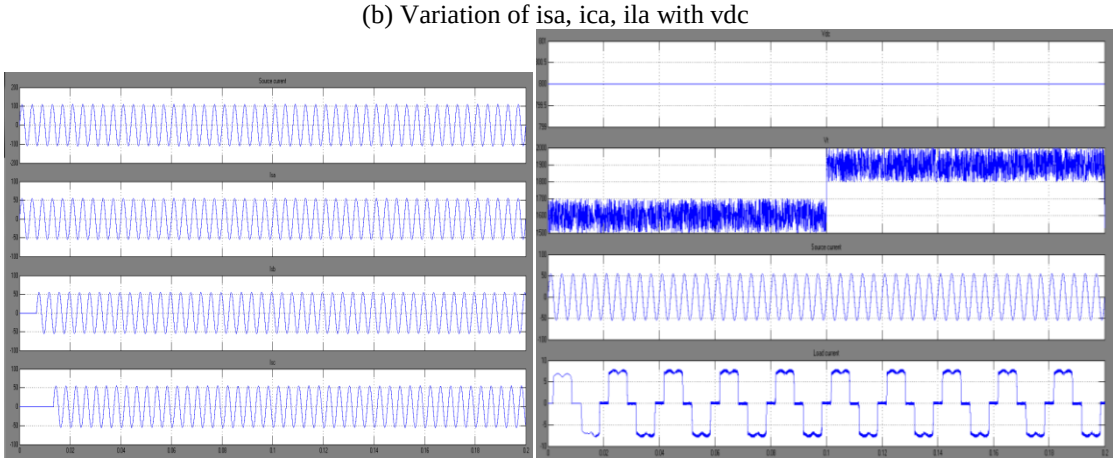


Fig.7 Dynamic performance of the DSTATCOM during unbalanced mixed loads (a) isa, isb, isc with Vab (b) Variation of isa, ica, ila with vdc



(a) **(b)**

Fig.8 Dynamic performance of DSTATCOM during unbalanced mixed loads at 225 V (a) isa, isb, isc with Vab (b) Variation of isa, ica, ila with vdc



(a) **(b)**

Fig.9 Dynamic performance of DSTATCOM during unbalanced nonlinear loads operation (a) isa, isb, isc with Vab (b) Variation of Vt, isa, and ila with vdc

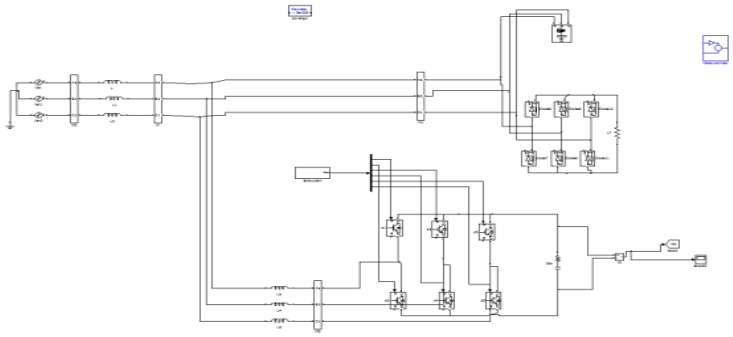
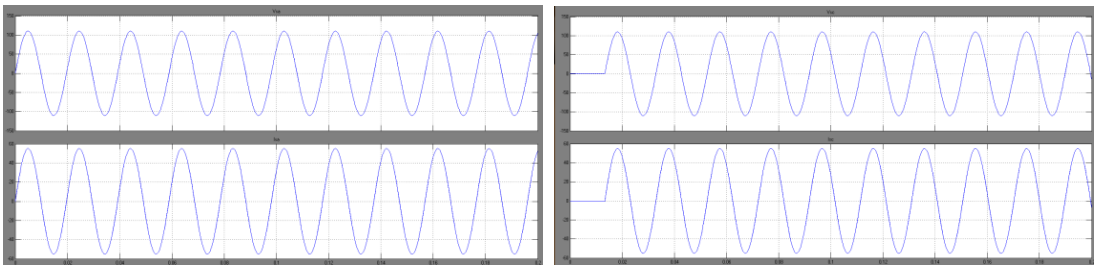
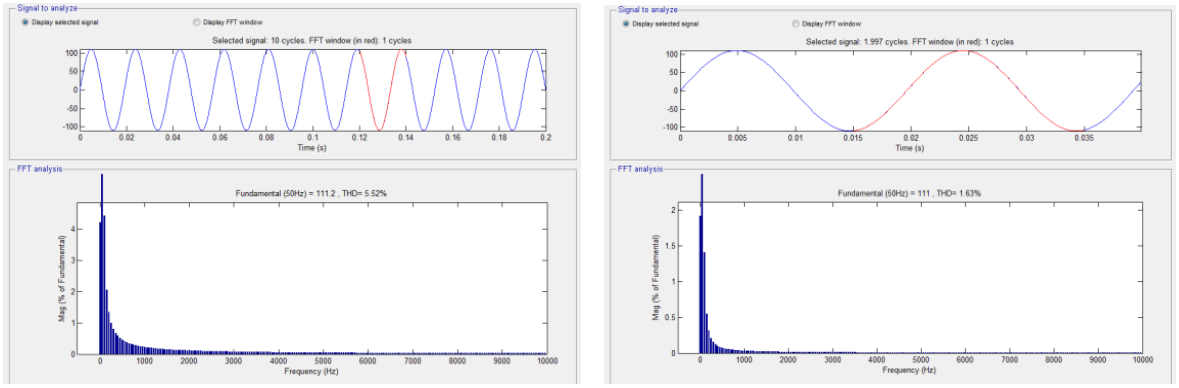


Fig.10 shows the Matlab/simulink model of proposed converter with pi & fuzzy controller



(a) (b)

Fig.11(a)-(b) Steady-state performance of DSTATCOM under linear lagging pf load in the ZVR mode vsa with isa , vsc with isc ,



(a) (b)

Fig.12(a)-(b) THD analysis of PI controller and fuzzy controller

VI. CONCLUSION

A DSTATCOM with five level CHB inverter is investigated. Mathematical model for single H-Bridge inverter is developed which can be extended to multi H-Bridge The source voltage, load voltage, source current, load current, power factor simulation results under non-linear loads. The performance of DSTATCOM and its control algorithm has been demonstrated for reactive power compensation, harmonics elimination, and load balancing in PFC and ZVR modes of operation under linear, nonlinear, and mixed loads. Test results have shown that the proposed control algorithm has a fast response for the extraction of fundamental components of load currents under noisy and distorted supply voltages. In all operating conditions, the THD of source current has been observed within an IEEE 519–1992 standard limit of 5%. The performance of DSTATCOM and its control has been found satisfactory under varying load conditions. The dc bus voltage of the DSTATCOM has also been regulated without any overshoot to the desired value under varying load conditions.

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